EXHIBIT 4

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

KIPB LLC, Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD.; SAMSUNG ELECTRONICS AMERICA, INC.; SAMSUNG SEMICONDUCTOR, INC.; SAMSUNG AUSTIN SEMICONDUCTOR, LLC; and QUALCOMM GLOBAL TRADING PTE. LTD., Defendants.	Case No. 2:19-cv-00056-JRG-RSP **JURY TRIAL DEMANDED**

DEFENDANTS' INVALIDITY CONTENTIONS

Defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, LLC, and Qualcomm Global Trading Pte. Ltd. (collectively, "Defendants"), by their attorneys, make these Invalidity Contentions concerning U.S. Patent No. 6,885,055 ("the '055 patent" or the "Asserted Patent") to KIPB LLC, formerly KAIST IP US LLC, ("Plaintiff" or "KIPB") in connection with the above-referenced action, pursuant to the Docket Control Order entered by the Court (Dkt. No. 29) and Local Patent Rule (P.R.) 3-3. The citation of prior art herein and the accompanying exhibits are not intended to reflect Defendants' claim construction contentions, which will be disclosed in due course in accordance with the Docket Control Order, and may instead reflect Plaintiff's apparent (and potentially erroneous) claim constructions based on its Infringement Contentions.

Defendants' Invalidity Contentions herein reflect Defendants' knowledge as of this early date in the present action. Defendants reserve the right, to the extent permitted by the Court and the applicable statutes and rules, to modify and/or supplement their Invalidity Contentions in response to becoming aware of additional prior art or information regarding prior art, any modification or supplementation of Plaintiff's Infringement Contentions, any claim construction by the Court, or as otherwise may be appropriate.

The Docket Control Order and the Patent Rules contemplate that these Invalidity Contentions would be prepared and served in response to Plaintiff's Infringement Contentions. However, Plaintiff's Infringement Contentions are insufficient because they lack proper and complete disclosure as to how Plaintiff contends that Defendants infringe the Asserted Claims. Due to Plaintiff's failure to provide proper and complete disclosure of its Infringement Contentions under P.R. 3-1, Defendants reserve the right to seek leave from the Court to amend these Invalidity Contentions should Plaintiff be allowed by the Court to amend its Infringement Contentions or its apparent claim constructions. Defendants also reserve the right to amend these Invalidity Contentions in light of positions that Plaintiff or its expert witnesses may assert concerning claim construction, infringement, and/or invalidity issues.

Defendants' Exhibits attached hereto cite to particular teachings and disclosures of the prior art as applied to features of the Asserted Claims. However, persons having ordinary skill in the art generally may view an item of prior art in the context of other publications, literature, products, and understanding. As such, the cited portions of prior art identified herein are exemplary only. Defendants may rely on the entirety of the prior art references listed herein, including un-cited portions of those prior art references, and on other publications and expert testimony shedding light on those prior art references, including as aids in understanding and

interpreting the cited portions, as providing context thereto, and as additional evidence that the prior art discloses a claim limitation.

Defendants will also rely on documents, products, testimony, and other evidence to establish bases for and motivations to make combinations of certain cited references that render the Asserted Claims obvious. Defendants may rely upon corroborating documents, products, testimony, and other evidence including materials obtained through further investigation and third-party discovery of the prior art identified herein, that describes the invalidating features identified in these contentions; evidence of the state of the art in the relevant time period (irrespective of whether such references themselves qualify as prior art to the Asserted Patent), including prior art listed on the face of the Asserted Patent and/or disclosed in the specification ("Admitted Prior Art"); and/or expert testimony to provide context to or aid in understanding the cited portions of the identified prior art.

The references discussed in the Exhibits herein disclose the elements of the Asserted Claims explicitly or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame. To the extent the attached claim charts cite to a reference for each element or limitation of an Asserted Claim, Defendants contend that such reference anticipates that claim. In addition, to the extent that the attached claim charts cite to additional references, Defendants contend, in the alternative, that the Asserted Claim is rendered obvious for the reasons set forth in the attached charts. To the extent suggested obviousness combinations are included in the attached claim charts, they are provided in the alternative to Defendants' anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not by itself anticipatory.

For purposes of these Invalidity Contentions, Defendants identify prior art references and provide element-by-element claim charts based, in part, on the apparent claim constructions advanced by Plaintiff in its Infringement Contentions. Nothing stated herein shall be treated as an admission or suggestion that Defendants agree with Plaintiff regarding either the scope of any of the Asserted Claims or the claim constructions advanced in the Infringement Contentions. For example, the claim term "Fin active region which is a wall-shape" has yet to be construed by the Court. Defendants' application of the prior art references to this claim term does not imply that Defendants accept Plaintiff's implicit claim constructions in its infringement contentions as to this claim term. As another example, the claim terms "a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer" and "a first oxide layer which is formed on the upper surface of said Fin active region with a thickness greater or equal to that of the gate oxide" have yet to be construed by the Court. Defendants' application of the prior art references to these claim terms does not imply that Defendants accept Plaintiff's implicit claim constructions in its infringement contentions as to these claim terms. Moreover, nothing in these Invalidity Contentions shall be treated as an admission that any Defendant's accused technology meets any limitations of the claims.

Pursuant to P.R. 3-3 and 3-4, Defendants have provided disclosures and related documents pertaining only to the Asserted Claims as identified by Plaintiff in its Infringement Contentions. *See* DEFTS_PA00000001 – DEFTS_PA00001634. Defendants will further supplement their P.R. 3-4 document production should they later find additional, responsive documents. Much of the art identified in the attached Exhibits reflect common knowledge and the state of the art prior to the priority date of the Asserted Patent. Further, Defendants incorporate by reference herein the entire prosecution history of *ex parte* reexamination control no. 90/014,227 filed on October 31, 2018

related to the Asserted Patent. To date, the United States Patent and Trademark Office has twice rejected the Asserted Claims of the Asserted Patent. *See* December 21, 2018 Order Granting *Ex Parte* Reexamination; *see also* February 13, 2019 Non-Final Office Action; *see also* June 18, 2019 Final Office Action. These rejections further support Defendants' Invalidity Contentions and the anticipation/obviousness of the Asserted Claims.

Each of the Asserted Claims[1] of the Asserted Patent is anticipated by and/or rendered obvious in view of one or more items of prior art identified herein, alone or in combination. Specific examples of this anticipation and obviousness, along with the motivation to combine the selected prior art, are set forth in Exhibit 6. The identification of obviousness combinations is not intended to be exhaustive, as there are many possible combinations of the references that one of ordinary skill in the art would have been motivated to make, and it is not practical to provide details of all such possible combinations.

I. Identification of Prior Art – Local Patent Rule 3-3(a)

> The identity of each item of prior art that allegedly anticipates each asserted claim or renders it obvious. Each prior art patent shall be identified by its number, country of origin, and date of issue. Each prior art publication must be identified by its title, date of publication, and where feasible, author and publisher.
>
> Prior art under 35 U.S.C. § 102(b) shall be identified by specifying the item offered for sale or publicly used or known, the date the offer or use took place or the information became known, and the identity of the person or entity which made the use or which made and received the offer, or the person or entity which made the information known or to whom it was made known.

P.R. 3-3(a).

[1] For reasons analogous to those identified herein, Defendants contend all *non-asserted* claims of the Asserted Patent are invalid as anticipated and/or obvious in view of the prior art or indefinite.

In addition to the prior art identified in the prosecution history of the Asserted Patent, Defendants intend to rely upon the prior art identified pursuant to P.R. 3-3(a) in the attached Exhibits in support of these Invalidity Contentions. In these contentions, including in the attached Exhibits, Defendants provide the full identity of each item of prior art, including: (1) each patent by its patent number, country of origin, and date of issue; (2) each non-patent publication by its title, date of publication, and, where feasible, author and publisher; (3) 35 U.S.C. § 102(b) prior art by the item offered for sale or publicly used or known, the date the offer or use took place or the information became known, and the identity of the person or entity which made the use or which made and received the offer, or the person or entity which made the information known or to whom it was made known; (4) 35 U.S.C. § 102(f) prior art by the name of the person(s) from whom and the circumstances under which the invention or any part of it was derived; and (5) 35 U.S.C. § 102(g) prior art by the identities of the person(s) or entities involved in and the circumstances surrounding the making of the invention before the patent applicant(s), based on currently available information.

Defendants' identification of patents and publications as prior art herein and in the attached claim charts under 35 U.S.C. §§ 102(a), (b), (e), and/or (g) and § 103 includes the publications themselves as well as the use of the products, devices, and systems described therein. Although Defendants' investigation continues, information available to date indicates that such products, devices, and systems were known and/or used in the country before the alleged invention of the claimed subject matter of the Asserted Claims, and/or were invented by another who did not abandon, suppress, or conceal, before the alleged invention of the claimed subject matter of the Asserted Claim. Upon information and belief, these prior art products, devices, systems, and their associated references anticipate and/or render obvious each of the Asserted Claims. Defendants

further intend to rely on inventor admissions concerning the scope of the prior art relevant to the Asserted Patent found in, *inter alia*, the prosecution history for the Asserted Patent and any related patents, patent applications, and/or re-examinations; any deposition testimony of the named inventor on the Asserted Patent; and the papers filed and any evidence submitted by Plaintiff in conjunction with this litigation.

As discovery is in its earliest stages, Defendants' prior art investigation, including third party discovery, is not yet complete. Defendants reserve the right to rely on evidence of invalidity obtained in the future. In addition, Defendants reserve the right to assert invalidity under 35 U.S.C. § 102(c) or (d) to the extent that further investigation and discovery yields information forming the basis for such claims.

A. Prior Art Patents

Defendants contend the following prior art patents anticipate or render obvious one or more Asserted Claims of the Asserted Patent under 35 U.S.C. §§ 102(a), (b), (e), and/or 35 U.S.C. § 103:

Country	Patent/Publication No.	Filing/Publication/ Issue Date	Inventor (et al.)
US	6,525,403	Filed Sep. 24, 2001 Issued Feb. 25, 2003	Inaba
US	2002/0011612	Filed Jul. 30, 2001 Published Jan. 31, 2002	Hieda
US	5,844,278	Filed Sep. 13, 1995 Issued Dec. 1, 1998	Mizuno
JP	2002-9289	Filed Jun. 20, 2000 Published Jan. 11, 2002	Ko
JP	H10-93093	Filed Sep. 18, 1996 Published Apr. 10, 1998	Yagishita
JP	H5-167043	Filed Apr. 24, 1992 Published Jul. 2, 1993	Yuzurihara
US	7,358,121	Filed Aug. 23, 2002 Issued Apr. 15, 2008	Chau
US	6,355,532	Filed Oct. 6, 1999 Issued Mar. 12, 2002	Seliskar

Country	Patent/Publication No.	Filing/Publication/ Issue Date	Inventor (et al.)
US	6,720,619	Filed Dec. 13, 2002 Issued Apr. 13, 2004	Chen
JP	H3-173175	Filed Dec. 1, 1989 Published Jul. 26, 2991 [sic]	Hisamoto
JP	H6-21452	Filed July 1, 1992 Published Jan. 28, 1994	Hikita
JP	PH7-86595	Filed Sep. 14, 1993, Published Mar. 31, 1995	Otsuki
US	6,475,869	Filed Feb. 26, 2001 Issued Nov. 5, 2002	Yu
US	5,849,624	Filed Jul. 30, 1996 Issued Dec. 15, 1998	Fazan
US	6,048,756	Filed Jun. 25, 1998 Issued Apr. 11, 2000	Lee
US	6,767,813	Filed Oct. 26, 2001 Issued Jul. 27, 2004	Lee
JP	2,633,001	Filed Jan. 30, 1989 Issued Apr. 25, 1997	Inokawa
US	5,115,289	Filed Aug. 5, 1991 Issued May 19, 1992	Hisamoto
JP	1996-139325	Filed Sept. 11, 1995 Published May 31, 1996	Mizuno
US	6,259,135	Filed Sept. 24, 1999 Issued July 10, 2001	Hsu
U.S.	2001-0052619	Filed Oct. 26, 1995 Published Dec. 20, 2001	S. Inoue
JP	2001-274383A	Filed Mar. 27, 2000 Published Oct. 5, 2001	Ozaki
JP	1990-125667	Filed Nov. 4, 1988 Published May 14, 1990	F. Inoue
US	5,391,506	Filed Jan. 27, 1993 Issued Feb. 21, 1995	Tada
US	6,642,090	Filed Jun. 3, 2002 Issued Nov. 4, 2003	Fried
JP	1989-8670	Filed July 1, 1987 Published Jan. 12, 1989	Hasegawa

B. Prior Art Publications

Defendants contend the following publications anticipate or render obvious one or more Asserted Claims of the Asserted Patent under 35 U.S.C. §§ 102(a), (b), and/or 35 U.S.C. § 103:

Publication Title	Date	Publisher	Author (s)
Process Development and Device Design for Continued MOSFET Scaling	Aug. 2001	Univ. of California, Berkeley	Lindert
Nanofabrication Technologies and Novel Device Structures for Nanoscale CMOS	Jan. 9, 2002	Univ. of California, Berkeley	Choi
High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices	Dec. 2001	IEEE	Kedzierski *et al.*
Super Self-Aligned Double-Gate (SSDG) MOSFETs Utilizing Oxidation Rate Difference and Selective Epitaxy	Dec. 1999	IEEE	Lee *et al.*
A Sub-40nm Body Thickness N-type FinFET	Jun. 2001	IEEE	Fried *et al.*
35 nm CMOS FinFETs	Jun. 2002	IEEE	Yang *et al.*
FinFET Scaling to 10nm Gate Length	2002	IEEE	Yu *et al.*
Silicon VLSI Technology – Fundamentals, Practice and Modeling, Chapter 11	2000	Prentice Hall	Plummer *et al.*
New Planar Self-Aligned Double-Gate Fully-Depleted P-MOSFET's Using Epitaxial Lateral Overgrowth (ELO) and Selectively Grown Source/Drain (S/D)	2000	IEEE	Su *et al.*
New Effects of Trench Isolated Transistor Using Side-Wall Gates	1987	IEEE	Hieda *et al.*
The Selective Epitaxial Growth of Silicon	1991	J. de Physique IV Colloque	Goulding
Selective epitaxial growth of silicon and some potential applications	Nov. 1990	IBM	Ginsberg *et al.*
Source/Drain Engineering for Sub-100 nm CMOS Using Selective Epitaxial Growth Technique	Dec. 2000	IEEE	Hokazono *et al.*
A New Three-Dimensional MOSFET Gate-Induced Drain Leakage Effect in Narrow Deep Submicron Devices	Dec. 1991	IEEE	Geissler *et al.*

Publication Title	Date	Publisher	Author (s)
Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation	Aug. 1987	IEEE	Yamabe *et al*.
SOI as a Mainstream IC Technology	Oct. 1998	IEEE	Adan *et al*.
Effect of Microscale Thermal Conduction on the Packing Limit of Silicon-on-Insulator Electronic Devices	Oct. 1992	IEEE	Goodson *et al*.
Historical overview of silicon crystal pulling development	Apr. 2000	Elsevier	Zulehner

C. Prior Art Public Use/Sales/Offers for Sale

As discovery is in its earliest stages, Defendants' prior art investigation, including third party discovery, is not yet complete. Defendants reserve the right to rely on evidence of invalidity obtained in the future as to any prior art public use/sales/offers for sale that may anticipate or render obvious one or more Asserted Claims of the Asserted Patent under 35 U.S.C. §§ 102(a) and/or (b) 35 U.S.C. § 103.

D. Prior Art under 35 U.S.C. § 102(f)

> Prior art under 35 U.S.C. § 102(f) shall be identified by providing the name of the person(s) from whom and the circumstances under which the invention or any part of it was derived.

P.R. 3-3(a).

Dr. Tai-Su Park worked with the named inventor of the '055 patent, Dr. Jong-Ho Lee, in advance of Dr. Lee filing the patent application that ultimately issued as the '055 patent. Dr. Park has testified in *KAIST IP US LLC v. Samsung Electronics Co., Ltd. et al.*, case no. 2-16-cv-01314 that he contributed to several aspects of the claimed invention.

Plaintiff may have in its possession, custody, or control information related to or pertaining to prior art under 35 U.S.C. § 102(f) but has yet to produce that information in discovery.

Defendants reserve the right to supplement these Invalidity Contentions if and when Plaintiff produces such information, after necessary analysis. Defendants will assert that the Asserted Patent is invalid under 35 U.S.C. § 102(f) in the event Defendants obtain evidence that the named inventor of the Asserted Patent did not alone invent the subject matter claimed in the Asserted Patent. Should Defendants obtain such evidence, they will provide the name of the person(s) from whom the invention or any part of it was derived and the relevant circumstances for such derivation.

E. Prior Art under 35 U.S.C. § 102(e) and 35 U.S.C. § 102(g)

> Prior art under 35 U.S.C. § 102(g) shall be identified by providing the identities of the person(s) or entities involved in and the circumstances surrounding the making of the invention before the patent applicant(s).

P.R. 3-3(a).

At present, Plaintiff has neither adequately alleged nor provided sufficient evidence of a conception date for the Asserted Patent earlier than the claimed priority date on the face of the Asserted Patent. In its Infringement Contentions, Plaintiff alleges that it does not claim priority to an earlier application. Should the Court permit Plaintiff to provide evidence of an earlier conception date, Defendants reserve the right to assert any § 102(a) prior art as § 102(e) and/or § 102(g) prior art. Moreover, on information and belief, the following references may provide evidence that prior to the alleged priority dates, the claimed invention was made in this country by another inventor who did not abandon, suppress, or conceal it.

Prior Art	Persons/Entities involved and circumstances surrounding the making of the invention
IBM FinFET devices	The IBM FinFET devices developed by researchers at IBM at least as of December

Prior Art	Persons/Entities involved and circumstances surrounding the making of the invention
	2001, as described in, for example, the publication: J. Kedzierski *et al*., "High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices," in International Electron Devices Meeting Technical Digest, pp. 19.5.1-19.5.4 (2001).
AMD FinFET devices	The AMD FinFET devices developed by researchers at AMD at least as of February 26, 2001, as described in, for example, the patent: U.S. Patent No. 6,475,869 to Yu.
Intel FinFET devices	The Intel FinFET devices developed by researchers at Intel at least as of August 23, 2002, as described in, for example, the patent: U.S. Patent No. 7,358,121 to Chau et al.
Toshiba FinFET devices	The Toshiba FinFET devices developed by researchers at Toshiba for example: U.S. Patent No. 5,844,278 to Mizuno et al., U.S. Patent No. 6,525,403 to Inaba et al., and JP Unexamined Patent Application Publication.
NEC FinFET devices	The NEC FinFET devices developed by researchers at NEC at least as of Jan. 11, 2002, as described in, for example, JP Unexamined Patent Application Publication 2002-9289 to Ko.
Sharp FinFET devices	The Sharp FinFET devices developed by researchers at Sharp as described in, for example, JP Unexamined Patent Application Publication H6-21452 to Hikita.
Samsung FinFET devices	The Samsung FinFET devices developed by researchers at Samsung at least as of Oct. 26, 2001 as described in, for example, U.S. Patent No. 6,767,813 to Lee *et al.*
Motorola FinFET devices	The Motorola FinFET devices developed by researchers at Motorola at least as of August 2001 as indicated in, for example, Lindert,

Prior Art	Persons/Entities involved and circumstances surrounding the making of the invention
	Process Development and Device Design for Continued MOSFET Scaling, Univ. of California, Berkeley (Page 132).
TSMC FinFET devices	The TSMC FinFET devices developed by researchers at TSMC at least as of August 2001 as indicated in, for example, Lindert, Process Development and Device Design for Continued MOSFET Scaling, Univ. of California, Berkeley (Page 132)..
MIT Microsystems Technology Laboratories devices ("MIT devices")	The MIT devices developed by researchers at MIT Microsystems Technology Laboratories at least as early as of December 1999, as described in, for example, J.-H. Lee *et al*., Super Self-Aligned Double-Gate (SSDG) MOSFETs Utilizing Oxidation Rate Difference and Selective Epitaxy, in International Electron Devices Meeting Technical Digest, pp. 71-74 (1999).
U.C. Berkeley FinFET devices ("U.C. Berkeley Devices")	The U.C. Berkeley devices developed by researchers at the University of California at Berkeley at least as early as of August 2001 as indicated in, for example, Lindert, Process Development and Device Design for Continued MOSFET Scaling, Univ. of California, Berkeley.

II. Local Patent Rules 3-3(b) and (c)

Whether each item of prior art anticipates each asserted claim or renders it obvious. If a combination of items of prior art makes a claim obvious, each such combination, and the motivation to combine such items must be identified.

A chart identifying where specifically in each alleged item of prior art each element of each asserted claim is found, including for each element that such party contends is governed by 35 U.S.C. § 112(6), the identity of the structure(s), act(s), or material(s) in each item of prior art that performs the claimed function.

In addition to the prior art disclosed in the Exhibits incorporated by reference herein, each of the Asserted Claims of the Asserted Patent is anticipated by and/or rendered obvious by prior art references identified above in **Sections I.A.** (list of prior art patents), **I.B.** (list of prior art publications), **I.C.** (list of prior art offered for sale or publicly used or known), and/or **I.E.** (list of prior invention prior art), alone or in combination. Generally, it would have been obvious to one of ordinary skill in the art to combine any of these references to arrive at the claimed invention. The combination of familiar elements according to known methods is obvious here because it yielded predictable results. Motivation to combine any two or more of the identified references comes from the fact that all of the references teach the design and/or fabrication and/or structure of semiconductor devices such as field effect transistors (*e.g.*, MOSFETs, FinFETs, MISFETs, etc.), and one would be motivated by considerations of efficiency, effectiveness, convenience, cost-savings, and accessibility to combine their teachings.

The Asserted Claims of the Asserted Patent are directed to obvious combinations of old and familiar steps or elements, each performing the same function it has long been known to perform, which only yield predictable results. Put another way, the claimed subject matter is obvious because it is nothing more than (i) combinations of prior art elements according to known methods to yield predictable results, (ii) simple substitutions of one known element for another to yield predictable results, (iii) applications of known techniques to known devices ready for improvement to yield predictable results, and/or (iv) obvious to try. One of skill in the art would have been motivated to either modify the prior art identified in the Invalidity Exhibits or to combine that prior art in the manner indicated, by, for example, their background knowledge, design incentives, effects of demands known to the design community, or other market forces, in particular the desire and need for more effective field effect transistor devices. Further, the prior

art discussed in this section all relates to the same general field of semiconductor device design and fabrication technology, including that related to field effect transistors (FETs) and addresses many of the same as well as different design and fabrication features of these devices. This would have further motivated one of skill in the art to combine those references. In view of the claimed subject matter's use of well-known components with recognized benefits, the common sense of those skilled in the art also would have served as a motivation to combine any of the identified references and demonstrates that the Asserted Claims of the Asserted Patent would be obvious.

Defendants have attached Exhibits containing claim charts identifying examples of prior art that anticipates and/or renders obvious each Asserted Claim of the Asserted Patent. Specifically, to the extent the attached claim charts cite to a reference for each element or limitation of an Asserted Claim, Defendants contend that such reference anticipates that claim. *See* Local Patent Rule 3-3(b) and (c). In addition, to the extent that the attached claim charts cite to additional references, Defendants contend, in the alternative, that the Asserted Claim is rendered obvious for the reasons set forth in the attached charts. To the extent suggested obviousness combinations are included in the attached claim charts, they are provided in the alternative to Defendants' anticipation contentions and are not to be construed to suggest that any reference included in the combinations is not by itself anticipatory.

Invalidity Charts
Ex. A -- U.S. Patent No. 6,525,403 to Inaba *et al*. (filed Sep. 24, 2001, issued Feb. 25, 2003) ("*Inaba*")
Ex. B -- U.S. Publication No. 2002/0011612 to Hieda (filed July 30, 2001, published Jan. 31, 2002) ("*Hieda*")
Ex. C -- U.S. Patent No. 5,844,278 to Mizuno *et al*. (filed May 26, 1995, issued Dec. 1, 1998) ("*Mizuno*")
Ex. D -- Japanese Unexamined Patent Application Pub. No. 2002-9289 to Ko (filed June 20, 2000; published Jan. 11, 2002) ("*Ko*")

Invalidity Charts
Ex. E -- J. Kedzierski *et al*., "High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices," IEEE 2001 International Electron Devices Meeting, Technical Digest (Cat. No.01CH37224), pp. 19.5.1-19.5.4 (Dec. 2001) ("*Kedzierski*")
Ex. F -- U.S. Patent No. 7,358,121 to Chau *et al*. (filed Aug. 23, 2002, issued Apr. 15, 2008) ("*Chau*")
Ex. G -- Y.K. Choi, "Nano-Fabrication Technologies and Novel Device Structures for Nanoscale CMOS," Doctoral Thesis, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, 2001 ("*Choi*")
Ex. H -- N. Lindert, "Process Development and Device Design for Continued MOSFET Scaling," Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Aug. 2001 ("*Lindert*")
Ex. I -- Japanese Unexamined Patent Application Publication H10-93093 to Yagishita *et al*. (published April 10, 1998) ("*Yagishita*")
Ex. J -- Japanese Unexamined Patent Application Publication H6-21452 to Hikita (published January 28, 1994) ("*Hikita*")
Ex. K -- U.S. Patent No. 6,767,813 to Lee *et al*. (filed Oct. 26, 2001; issued Jul. 27, 2004) ("*Lee '813*")
Ex. L -- Japanese Unexamined Patent Application Publication H5-167043 to Yuzurihara *et al.* (published July 2, 1993) ("*Yuzurihara*")
Ex. M -- Japanese Patent No. 2,633,001 to Inokawa (filed Jan 30, 1989; issued Apr. 25, 1997) ("*Inokawa*")
Ex. N -- U.S. Patent No. 5,115,289 to Hisamoto *et al*. (filed Aug. 5, 1991; issued May 19, 1992) ("*Hisamoto*")
Ex. O -- Japanese Unexamined Patent Application Publication 1996-139325 to Mizuno *et al.* (published May 31, 1996) ("*JP Mizuno*")
Ex. P -- U.S. Patent No. 6,259,135 to Hsu *et al.* (filed Sep. 24, 1999) ("*Hsu*")
Ex. Q -- U.S. Patent Publication No. 2001/0052619 to S. Inoue *et al*. (filed Oct. 26, 1995 and published Dec. 20, 2001) ("*S. Inoue*")
Ex. R -- Japanese Published Patent Application No. 2001-274383A to Ozaki *et al*. (published Oct. 5, 2001) ("*Ozaki*")
Ex. S -- Japanese Published Patent Application No. 1990-125667 to Fumihiko Inoue (published May 14, 1990) ("*F. Inoue*");
Ex. T -- U.S. Patent No. 5,391,506 to Tada *et al.* (filed Jan. 27, 1993 and issued Feb. 21, 1995) ("*Tada*");
Ex. U -- U.S. Patent No. 6,642,090 to Fried *et al*. (filed Jun. 3, 2002 and issued Nov. 4, 2003) ("*Fried*")
Ex. V -- Japanese Published Patent Application No. 1989-8670 to Hasegawa ("Hasegawa")

To the extent not identified above in Section I, Defendants identify all references listed in the Invalidity Charts table as prior art references anticipating and/or rendering obvious one or more claims of the Asserted Patent.

To the extent that Plaintiff contends that any one of the primary references does not disclose one or more elements of the Asserted Claims, it would have been obvious to combine the primary references in the Invalidity Charts with one or more of the below exhibits, collectively the "Obviousness Exhibits," as discussed more fully in each Invalidity Chart and Obviousness Exhibit.

All of the Asserted Claims of the Asserted Patent are anticipated, expressly or inherently, and therefore fail to meet one or more of the requirements for patentability, as detailed in the Invalidity Charts. Additionally, and in the alternative, the Asserted Claims of the Asserted Patent are obvious in view of the state of the art at the pertinent time (including Admitted Prior Art) alone and/or in combination with the references described in the above-referenced Exhibits as well as the references and disclosures described in the Obviousness Exhibits below. The alleged "inventions" claimed in the Asserted Claims of the Asserted Patent would have been obvious because the prior art, common knowledge, and the nature of the problems, viewed through the eyes of a person ordinarily skilled in the art, suggested the claimed elements. A person of ordinary skill in the relevant fields would have possessed knowledge and skills rendering him or her capable of combining the prior art references with knowledge in the field and common sense. Moreover, the Asserted Claims represent well-known combinations of familiar and pre-existing elements, yielding only predictable results. Additional reasons that a person of ordinary skill in the art would have been motivated to combine the identified prior art are provided in the Exhibits attached hereto.

In addition to the specific combinations of prior art and the specific combinations of groups of prior art disclosed, Defendants will rely on any other combination of any prior art references disclosed herein. Defendants further will rely upon combinations disclosed within the prosecution history of the references cited herein. The obviousness combinations set forth in these contentions

reflect Defendants' present understanding of the scope of the claims that Plaintiff appears to be asserting, and are not concessions to Plaintiff's interpretation of the patent claims. Defendants will amend or supplement these contentions regarding anticipation and/or obviousness of the Asserted Claims as appropriate under the applicable Rules, including in response to further information from Plaintiff or information discovered during discovery. Plaintiff has not identified what elements or combinations it alleges were not known to one of ordinary skill in the art at the pertinent time. Therefore, for any claim limitation that Plaintiff alleges is not disclosed in a particular prior art reference, Defendants reserve the right to assert that any such limitation is either inherent in the disclosed reference or obvious to one of ordinary skill in the art at the pertinent time in light of the same, or that the limitation is disclosed in another of the references disclosed above and in combination would have rendered the Asserted Claim obvious.

In an effort to focus the issues, Defendants have cited representative portions of the identified references, even where a reference may contain additional support for a particular claim element. Defendants note that a person of ordinary skill in the art generally reads a prior art reference as a whole, in the context of other publications and literature. Thus, to understand and interpret any specific statement or disclosure within a prior art reference, such person would rely on other information within the reference, along with other publications and their general scientific knowledge. Hence, Defendants will rely on the cited prior art references in their entirety, including the un-cited portions.

Additionally, any reference or combination of references that anticipates or renders obvious an asserted independent claim also renders obvious any Asserted Claim dependent on that independent claim because every element of each dependent claim was known by a person of ordinary skill at the time of the alleged invention, and/or it would have been obvious to combine

known elements with the independent claims at least as a matter of common sense and routine innovation.

Obviousness Exhibits
Ex. 1 -- Defendants' Invalidity Contentions for the Obviousness of the Bulk Silicon Substrate Claims • U.S. Patent No. 6,525,403, filed Sep. 24, 2001, issued Feb. 25, 2003 to *Inaba et al*. ("*Inaba*"); • U.S. Patent Publication No. 2002/0011612, filed July 30, 2001, published Jan. 31, 2002 to *Hieda et al*. ("*Hieda*"); • Japanese Unexamined Patent Application Publication. JP2002-009289 to *Ko* ("*Ko*"); • U.S. Patent No. 5,844,278 to *Mizuno et al*. (filed May 26, 1995, issued Dec. 1, 1998) ("*Mizuno*"); • Japanese Unexamined Patent Application Publication. H6-21452 to *Hikita* ("*Hikita*"); • U.S. Patent No. 6,767,813 to Lee *et al*. (filed Oct. 26, 2001; issued Jul. 27, 2004) ("*Lee '813*"); • Japanese Unexamined Patent Application Publication H5-167043 to *Yuzurihara et al.* (published July 2, 1993) ("*Yuzurihara*"); • K. Hieda *et al*., "New Effects of Trench Isolated Transistor Using Side-Wall Gates," in International Electron Devices Meeting Tech. Dig., 1987, pp. 736–739 ("*Hieda IEDM*"); • Japanese Unexamined Patent Application Publication H10-93093 to *Yagishita et al.* ("*Yagishita*"); • Adan *et al*., "SOI as a Mainstream IC Technology," Proc. Of the 1998 IEEE Int'l. SOI Conference, October 1998 ("*Adan*"); • Goodson *et al*., "Effect of Microscale Thermal Conduction on the Packing Limit of Silicon-on-Insulator Electronic Devices," IEEE Trans. on Components, Hybrids and Manufacturing Techn., vol. 15, no. 5, October 1992 ("*Goodson*"); • Zulehner, "Historical overview of silicon crystal pulling development," Materials Science & Engineering B73 (2000), pp. 7-15 ("*Zulehner*"); • Japanese Patent No. 2,633,001 filed Jan 30, 1989; issued Apr. 25, 1997 to *Inokawa et al*. ("*Inokawa*"); • U.S. Patent No. 5,115,289 filed Aug. 5, 1991; issued May 19, 1992 to *Hisamoto et al*. ("*Hisamoto*"); • Japanese Published Patent Application No. 1996-139325 published May 31, 1996 to *Mizuno et al*. ("*JP Mizuno*"); • U.S. Patent No. 6,259,135 filed Sep. 24, 1999 to *Hsu et al*. ("*Hsu*"); • U.S. Patent Publication No. 2001/0052619 filed Oct. 26, 1995 and published Dec. 20, 2001 to *S. Inoue et al*. ("*S. Inoue*"); • Japanese Published Patent Application No. 2001-274383A published Oct. 5, 2001 to *Ozaki et al*. ("*Ozaki*"); • Japanese Published Patent Application No. 1990-125667 published May 14, 1990 to Fumihiko Inoue ("*F. Inoue*");

Obviousness Exhibits
• U.S. Patent No. 5,391,506 filed Jan. 27, 1993 and issued Feb. 21, 1995 to *Tada et al*. ("*Tada*"); • U.S. Patent No. 6,642,090 filed Jun. 3, 2002 and issued Nov. 4, 2003 to *Fried et al*. ("*Fried*"); • Japanese Published Patent Application No. 1989, 8670 to Hasegawa ("*Hasegawa*"); • The '055 patent, which admits that the use of bulk silicon substrates was known in the prior art.
Ex. 2 -- Defendants' Invalidity Contentions for the Obviousness of a Gate Oxide Layer and a First Oxide Layer Claims • U.S. Patent No. 6,525,403, filed Sep. 24, 2001, issued Feb. 25, 2003 to *Inaba et al*. ("*Inaba*"); • U.S. Patent Publication No. 2002/0011612, filed July 30, 2001, published Jan. 31, 2002 to *Hieda et al*. ("*Hieda*"); • Japanese Unexamined Patent Application Publication. JP2002-009289 to *Ko* ("*Ko*"); • U.S. Patent No. 5,844,278 to *Mizuno et al*. (filed May 26, 1995, issued Dec. 1, 1998) ("*Mizuno*"); • Japanese Unexamined Patent Application Publication H10-93093 to *Yagishita et al.* ("*Yagishita*"); • F.-L. Yang *et al*., "35 nm CMOS FinFETs," in Symp. VLSI Technology Tech. Dig., 2002, pp. 104–105 ("*Yang*"); • B. Yu *et al*., "FinFET Scaling to 10nm Gate Length," in International Electron Devices Meeting Tech. Dig., 2002, pp. 251–54 ("*Yu IEDM*"); • Japanese Patent No. 2,633,001 filed Jan 30, 1989; issued Apr. 25, 1997 to *Inokawa et al*. ("*Inokawa*"); • Japanese Published Patent Application No. 1996-139325 published May 31, 1996 to *Mizuno et al*. ("*JP Mizuno*"); • U.S. Patent No. 6,642,090 filed Jun. 3, 2002 and issued Nov. 4, 2003 to *Fried et al*. ("*Fried*"); • U.S. Patent No. 5,115,289 filed Aug. 5, 1991; issued May 19, 1992 to *Hisamoto et al*. ("*Hisamoto*"); • U.S. Patent No. 6,259,135 filed Sep. 24, 1999 to *Hsu et al*. ("*Hsu*"); • U.S. Patent Publication No. 2001/0052619 filed Oct. 26, 1995 and published Dec. 20, 2001 to *S. Inoue et al*. ("*S. Inoue*"); • Japanese Published Patent Application No. 2001-274383A published Oct. 5, 2001 to *Ozaki et al*. ("*Ozaki*"); • Japanese Published Patent Application No. 1990-125667 published May 14, 1990 to Fumihiko Inoue ("*F. Inoue*"); • U.S. Patent No. 5,391,506 filed Jan. 27, 1993 and issued Feb. 21, 1995 to *Tada et al*. ("*Tada*"); • Japanese Published Patent Application No. 1989, 8670 to *Hasegawa* ("*Hasegawa*"); • JP Patent Publication No. H6-21452, filed July 1, 1992, published Jan. 28, 1994 to *Hikita* ("*Hikita*");

Obviousness Exhibits
• U.S. Patent No. 6,767,813 to Lee *et al*. (filed Oct. 26, 2001; issued Jul. 27, 2004) ("*Lee '813*"); • Choi, *Nanofabrication Technologies and Novel Device Structures for Nanoscale CMOS*, Univ. of California, Berkeley, published Jan. 9, 2002 ("*Choi*"); • Japanese Unexamined Patent Application Publication H5-167043, published July 2, 1993 to *Yuzurihara et al.* ("*Yuzurihara*"); • N. Lindert, "Process Development and Device Design for Continued MOSFET Scaling," Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, published 2001 ("*Lindert*"); • J. Kedzierski *et al*., "High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices," in International Electron Devices Meeting Tech. Dig., 2001, pp. 19.5.1-19.5.4 ("*Kedzierski*"); • U.S. Patent No. 7,358,121, filed Aug. 23, 2002 and issued Apr. 15, 2008 to *Chau et al*. ("*Chau*"). • The '055 patent, which admits that double-gate FinFET having a gate oxide layer and a first oxide layer was known in the prior art.
Ex. 3 -- Defendants' Invalidity Contentions for the Obviousness of the Contact Region and Metal Layer Claims • U.S. Patent No. 6,525,403, filed Sep. 24, 2001, issued Feb. 25, 2003 to *Inaba et al*. ("*Inaba*"); • U.S. Patent Publication No. 2002/0011612, filed July 30, 2001, published Jan. 31, 2002 to *Hieda et al*. ("*Hieda*"); • Japanese Unexamined Patent Application Publication. JP2002-009289 to *Ko* ("*Ko*"); • U.S. Patent No. 5,844,278 to *Mizuno et al*. (filed May 26, 1995, issued Dec. 1, 1998) ("*Mizuno*"); • U.S. Patent No. 7,358,121, filed Aug. 23, 2002, issued Apr. 15, 2008 to *Chau et al*. ("*Chau*"); • Japanese Unexamined Patent Application Publication H5-167043 to *Yuzurihara et al.* (published July 2, 1993) ("*Yuzurihara*"); • Japanese Unexamined Patent Application Publication H10-93093 to *Yagishita et al.* ("*Yagishita*"); • F.-L. Yang *et al*., "35 nm CMOS FinFETs," in Symp. VLSI Technology Tech. Dig., 2002, pp. 104–105 ("*Yang*"); • J.-H. Lee *et al*., Super Self-Aligned Double-Gate (SSDG) MOSFETs Utilizing Oxidation Rate Difference and Selective Epitaxy, in IEDM Tech. Dig., 1999, pp. 71–74 ("*Lee*"); • U.S. Patent No. 6,475,869 to *Yu* (filed Feb. 26, 2001, issued Nov. 5, 2002) ("*Yu*"); • B. Yu *et al*., "FinFET Scaling to 10nm Gate Length," in International Electron Devices Meeting Tech. Dig., 2002, pp. 251–54 ("*Yu IEDM*"); • T. Su *et al*., "New Planar Self-Aligned Double-Gate Fully-Depleted P-MOSFET's Using Epitaxial Lateral Overgrowth (ELO) and Selectively Grown Source/Drain (S/D)," in IEEE Int. SOI Conf., 2000, pp. 110–111 ("*Su*");

Obviousness Exhibits
• J. Plummer *et al*., Silicon VLSI Technology – Fundamentals, Practice and Modeling, Chapter 11, (2000) ("*Plummer*"); • Japanese Patent No. 2,633,001 filed Jan 30, 1989; issued Apr. 25, 1997 to *Inokawa et al*. ("*Inokawa*"); • U.S. Patent No. 5,115,289 filed Aug. 5, 1991; issued May 19, 1992 to *Hisamoto et al*. ("*Hisamoto*"); • Japanese Published Patent Application No. 1996-139325 published May 31, 1996 to *Mizuno et al*. ("*JP Mizuno*"); • U.S. Patent No. 6,259,135 filed Sep. 24, 1999 to *Hsu et al*. ("*Hsu*"); • U.S. Patent Publication No. 2001/0052619 filed Oct. 26, 1995 and published Dec. 20, 2001 to *S. Inoue et al*. ("*S. Inoue*"); • U.S. Patent No. 6,642,090 filed Jun. 3, 2002 and issued Nov. 4, 2003 to *Fried et al*. ("*Fried*"); • Japanese Published Patent Application No. 1989, 8670 to *Hasegawa* ("*Hasegawa*"); • The '055 patent, which admits that double-gate FinFET devices being electrical devices and including metal layers, was known in the prior art.
Ex. 4 -- Defendants' Invalidity Contentions for the Obviousness of the FinFET Physical Dimensions Claims • U.S. Patent No. 6,525,403, filed Sep. 24, 2001, issued Feb. 25, 2003 to *Inaba et al*. ("*Inaba*"); • U.S. Patent Publication No. 2002/0011612, filed July 30, 2001, published Jan. 31, 2002 to *Hieda et al*. ("*Hieda*"); • Japanese Unexamined Patent Application Publication. JP2002-009289 to *Ko* ("*Ko*"); • J. Kedzierski *et al*., "High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices," IEEE 2001 International Electron Devices Meeting, Technical Digest (Cat. No.01CH37224), pp. 19.5.1-19.5.4 (Dec. 2001) ("*Kedzierski*"); • U.S. Patent No. 5,844,278 to *Mizuno et al*. (filed May 26, 1995, issued Dec. 1, 1998) ("*Mizuno*"); • JP Patent Publication No. H6-21452, filed July 1, 1992, published Jan. 28, 1994 to *Hikita* ("*Hikita*"); • U.S. Patent No. 6,767,813 to Lee *et al*. (filed Oct. 26, 2001; issued Jul. 27, 2004) ("*Lee '813*"); • Choi, *Nanofabrication Technologies and Novel Device Structures for Nanoscale CMOS*, Univ. of California, Berkeley, published Jan. 9, 2002 ("*Choi*"); • Japanese Unexamined Patent Application Publication H10-93093 to *Yagishita et al.* ("*Yagishita*"); • Japanese Unexamined Patent Application Publication H5-167043 to *Yuzurihara et al.* (published July 2, 1993) ("*Yuzurihara*"); • U.S. Patent No. 6,475,869 to *Yu* (filed Feb. 26, 2001, issued Nov. 5, 2002) ("*Yu*"); • B. Yu *et al*., "FinFET Scaling to 10nm Gate Length," in International Electron Devices Meeting Tech. Dig., 2002, pp. 251–54 ("*Yu IEDM*");

Obviousness Exhibits
• F.-L. Yang *et al*., "35 nm CMOS FinFETs," in Symp. VLSI Technology Tech. Dig., 2002, pp. 104–105 ("*Yang*"); • D.M. Fried *et al*., "A sub-40nm body thickness n-type FinFET," Device Research Conference, June 2001, pp. 24-25 ("*Fried #2*"); • Japanese Patent No. 2,633,001 filed Jan 30, 1989; issued Apr. 25, 1997 to *Inokawa et al*. ("*Inokawa*"); • U.S. Patent No. 5,115,289 filed Aug. 5, 1991; issued May 19, 1992 to *Hisamoto et al*. ("*Hisamoto*"); • Japanese Published Patent Application No. 1996-139325 published May 31, 1996 to *Mizuno et al*. ("*JP Mizuno*"); • U.S. Patent No. 6,259,135 to *Hsu et al*. ("*Hsu*"); • U.S. Patent Publication No. 2001/0052619 filed Oct. 26, 1995 and published Dec. 20, 2001 to *S. Inoue et al*. ("*S. Inoue*"); • Japanese Published Patent Application No. 2001-274383A published Oct. 5, 2001 to *Ozaki et al*. ("*Ozaki*"); • Japanese Published Patent Application No. 1990-125667 published May 14, 1990 to *Fumihiko Inoue* ("*F. Inoue*"); • U.S. Patent No. 5,391,506 filed Jan. 27, 1993 and issued Feb. 21, 1995 to *Tada et al*. ("*Tada*"); • U.S. Patent No. 6,642,090 filed Jun. 3, 2002 and issued Nov. 4, 2003 to *Fried et al*. ("*Fried*"); • Japanese Published Patent Application No. 1989, 8670 to *Hasegawa* ("*Hasegawa*"); • The '055 patent, which admits that double-gate FinFET devices and the dimensions of such devices, including Fin active region widths between 4 nm and 100 nm, were known in the prior art.
Ex. 5 -- Defendants' Invalidity Contentions for the Obviousness of the Fin Active Region Top Chamfered Corners Claims • U.S. Patent Publication No. 2002/0011612, filed July 30, 2001, published Jan. 31, 2002 to *Hieda et al*. ("*Hieda*"); • U.S. Patent No. 5,844,278 to *Mizuno et al*. (filed May 26, 1995, issued Dec. 1, 1998) ("*Mizuno*"); • U.S. Patent No. 6,355,532, filed Oct. 6, 1999, issued Mar. 12, 2002 to *Seliskar et al*. ("*Seliskar*"); • U.S. Patent No. 6,720,619 filed December 13, 2002 and issued April 13, 2004 to *Chen et al*. ("*Chen*"); • JP Published Patent Application No. 2001-274383A published Oct. 5, 2001 to *Ozaki et al*. ("*Ozaki*"); • JP Patent Publication No. PH7-86595, filed Sep. 14, 1993, published Mar. 31, 1995 to *Otsuki* ("*Otsuki*"); • JP Published Patent Application No. H3-173175, filed Dec. 1, 1989, published Jul. 26, 2991 [sic] to *Hisamoto et al*. ("*Hisamoto #2*"); • U.S. Patent No. 5,849,624 to *Fazan et al*. ("*Fazan*");

Obviousness Exhibits
• Geissler *et al*., "A New Three-Dimensional MOSFET Gate-Induced Drain Leakage Effect in Narrow Deep Submicron Devices," in International Electron Devices Meeting Tech. Dig., 1991, pp. 839–842 ("*Geissler*"); • Yamabe *et al*., Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation, IEEE Trans. on Electron Devices, vol. ED-34, no. 8, August 1987 ("*Yamabe*").

The combinations of references demonstrating the obviousness of the Asserted Claims of the Asserted Patent under 35 U.S.C. § 103 are listed in Exhibit 6.

In addition to the specific combinations of prior art references and the motivations to combine discussed in Exhibit 6, one would be motivated to address the alleged problems or achieve the purported objectives identified in the "Background" sections of the Asserted Patent. Moreover, the Asserted Patent admits that numerous claim requirements[2] were well known at the time of the alleged invention, including "double-gate" devices, "FinFETs," "double-gate FinFET devices," "bulk silicon substrates," "gate oxide layers," "gates," "source/drain regions," "metal layers," "self-aligned" devices, and claim requirements substantially similar to the above. *See, e.g.*, '055 patent at 1:5–4:7. In fact, the '055 patent admits that a double-gate FinFET device having many of the claimed features were also well-known in the prior art. In particular, the '055 patent admits that "a double-gate FinFET device" having: "a bulk silicon substrate" (*see, e.g.*, *id*. Fig. 2b (element 2a)), "Fin active region," (*see, e.g.*, *id*. at Fig. 2b (element 34)) "a gate oxide layer . . . formed on both side-walls of the Fin active region" (*see, e.g.*, *id*. at Fig. 2b (element 12)), a "second oxide layer" (*see, e.g.*, *id*. Figs 2b (element 10)), a "first oxide layer which is formed on the upper

[2] As stated below, Defendants believe some of these elements to be indefinite and do not concede they are adequately disclosed or delineated in the Asserted Patent, but simply that the Asserted Patent admits these elements (whatever they may be) are not novel. Furthermore, this list is only illustrative, and Defendants do not concede that other claim elements not listed here were not expressly or implicitly admitted by the patentees to be present in the prior art.

surface of . . . Fin active region with a thickness greater or equal to that of the gate oxide" layer (*see, e.g.*, *id*. at Fig., 2b (element 6)), a "gate which is formed on . . . first and second oxide layers" (*see, e.g.*, *id*. at Fig. 2b (element 16)), was known in the prior art.

For example, the '055 patent specification discloses that a "double-gate device structure has emerged as the most appropriate device structure for reducing the channel length of a CMOS device below 25 nm or less." *Id*. at 1:65–67.

The '055 patent specification further admits that double-gate FinFET devices were conventional:

> FIG. 2 a and FIG. 2 b are perspective views which show the conventional structure of a Fin FET device which are represented by semi-transparent and shaded, respectively.

'055 patent at 4:59–61; *see also id*. at 2:37–39.

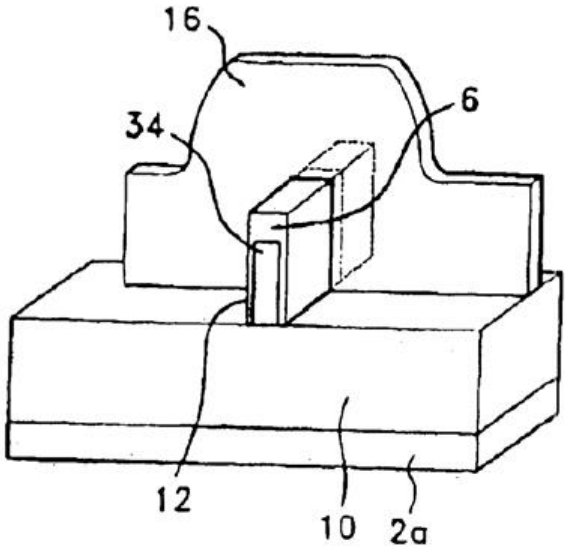

Fig. 2a

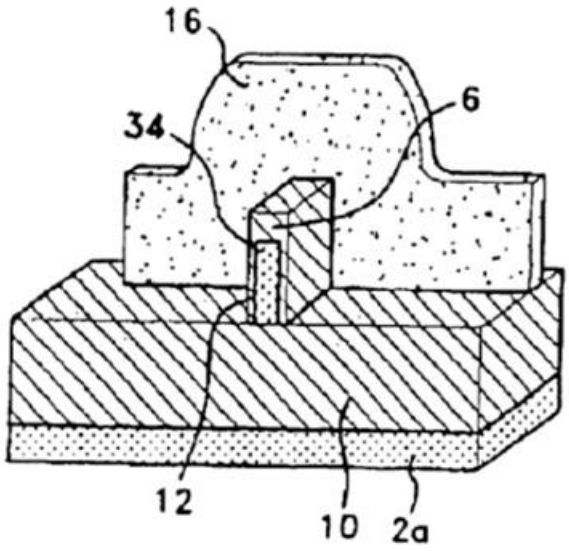

Fig. 2b

Id. at Figs. 2a, 2b.

The specification of the '055 patent admits that the conventional double-gate FinFET device (as shown in Figs. 2a and 2b) includes a silicon substrate 2a, oxide layers 6 and 10, a gate oxide layer 12, a channel 34, and gate electrode 16 formed on both sides of the channel 34. *See, e.g.*,

> FIG. 2 a and FIG. 2 b represent the same structures where FIG. 2 a is semi-transparent and FIG. 2 b is shaded. Here, the structure and the current flow direction correspond to those of FIG. 1 c. The short channel effects can significantly be reduced by forming a gate electrode 16 at both (top/bottom) sides of the channel 34. A silicon substrate 2 a of SOI wafer, oxide layers 6, 10 and a gate oxide layer 12 are shown in FIG. 2 a.

Id. at 2:43–47. The specification of the '055 patent further admits that there are other features of the conventional FinFET device, but which it "omit[s] for simplicity."

> FIG. 2 shows the essential parts of a conventional FinFET structure where the metal layer for wiring was omitted for simplicity.

Id. at 2:37–39.

According to the '055 patent, the above-described conventional double-gate FinFET structure has certain disadvantages. *Id*. at 3:64–4:19, 3:64–65, 4:1–4, 4:4–7. The '055 patent allegedly solves these problems by simply connecting the channel region 34 to the bulk substrate 2a in the conventional double-gate FinFET device. For instance, the '055 patent discloses, with reference to Figs. 3a–b, a purportedly novel double-gate FinFET device having a Fin active region 4 (in which the channel and source/drain regions are formed) connected to the bulk silicon substrate 2b. *Id*. at 4:10-19, Figs. 3a-3b; *see also id*. at 5:36-52. By doing so, it is purported that the problems associated with the conventional double-gate FinFET device are resolved. *Id*.; *see also id*. at 6:16-25. Figs. 2b (conventional FinFET) only differs from Fig. 3b (purportedly novel FinFET of the '055 patent) simply in that the bulk silicon substrate 2b is connected to the Fin active region 4 as shown in Fig. 3b. *See, e.g.*, *id*. at 6:16–25 (describing this difference between

Figs. 2b and 3b), Figs. 2a–2b, 3a–3b.). The FinFET devices of Fig. 2b and Fig. 3b are otherwise identical.

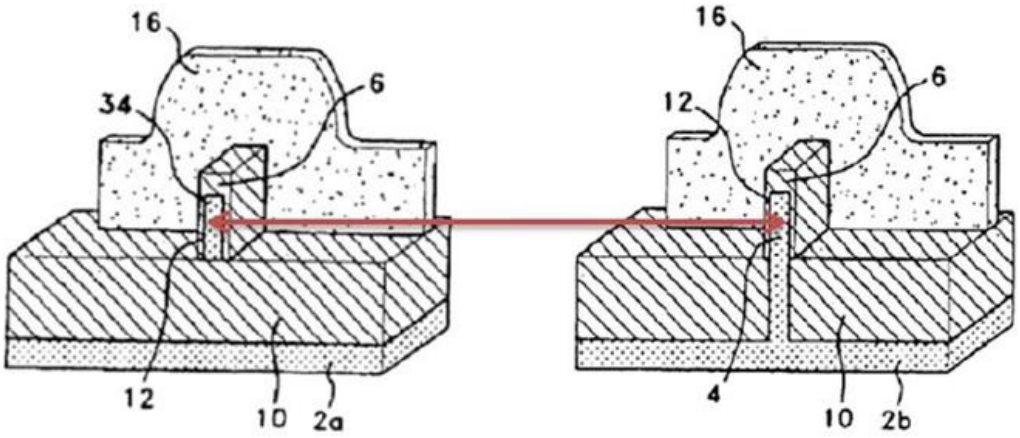

Fig. 2b

CONVENTIONAL FINFET

Fig. 3b

PURPORTEDLY NEW FINFET

Id. at Figs. 2b, 3b (annotated).

Additional obviousness combinations of the prior art references identified herein are possible, and Defendants reserve the right to use any such combination(s) in this litigation. In particular, Defendants are currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the claims at issue are not disclosed in the art identified by Defendants as anticipatory. To the extent that an issue arises with any such limitation, Defendants reserve the right to identify other references that would have made obvious the additional allegedly missing limitation to the disclosed device or method of operation.

III. Local Patent Rule 3-3(d)

> Any grounds of invalidity based on indefiniteness under 35 U.S.C. § 112(2) or enablement or written description under 35 U.S.C. § 112(1) of any of the Asserted Claims.

In addition to and including the grounds of invalidity set forth in the Invalidity Contentions incorporated by reference herein, Defendants contend that the Asserted Claims of the Asserted Patent are invalid under 35 U.S.C. § 112, paragraphs one and/or two for at least the following reasons.

A. Indefiniteness under 35 U.S.C. § 112, ¶ 2

The Asserted Claims of the Asserted Patent are invalid because they fail to meet the "definiteness" requirement of 35 U.S.C. § 112, ¶ 2, which states that the claims must "particularly point[] out and distinctly claim[] the subject matter which the inventor [] regards as [the] invention." In particular, the Asserted Claims of the Asserted Patent are indefinite because of at least the following terms or phrases:

Claim	Term
All Asserted Claims	"a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate;"
All Asserted Claims	"a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region;"
All Asserted Claims	"the upper surface of Fin active region"
All Asserted Claims	"a contact region and a metal layer which are formed at said source/drain and gate contact region,"
All Asserted Claims	"a first oxide layer which is formed on the upper surface of said Fin active region with a thickness greater or equal to that of the gate oxide;"
Asserted Claims 1-6, 11, 12, 15-17	"the thickness of said gate oxide layer"
Asserted Claims 1-6, 11, 12, 15-17	"the thickness of said first oxidation layer"
Asserted Claims 2, 16, 17	"the width of said Fin active region"

Claim	Term
Asserted Claims 3, 4	"the height of said Fin active region"
Asserted Claim 5	"the parasitic capacitance between said gate and bulk silicon substrate is reduced by selecting the thickness of said second oxidation layer to be between 20 nm and 800 nm."
Asserted Claim 6	"the contact resistance is reduced by selecting the size of a contact region which is in contact with said metal layer to be greater than the width of said Fin active region and/or the length of said gate."
Asserted Claim 11	"said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to 50 nm above the reference level."
Asserted Claim 12	"said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to −50 nm below the reference level."
Asserted Claim 13	"the resistance of said Fin active region is reduced by enlarging the width of said Fin active region within the oxidation layer as it approaches the bulk silicon substrate."
Asserted Claim 15	"the two top corners of said Fin active region are chamfered through an oxidation and etching, or (and) annealing process in a hydrogen atmosphere."

To the extent other Asserted Claims contain one of these terms or phrases, either directly or through being a dependent claim of a claim that does, those Asserted Claims of the Asserted Patent are invalid under 35 U.S.C. § 112, ¶ 2.

The claims are indefinite as they fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.

B. Lack of Enablement under 35 U.S.C. §112, ¶ 1

The Asserted Claims of the Asserted Patent are invalid because they fail to meet the "enablement" requirement of 35 U.S.C. § 112, ¶ 1, because the Asserted Patent does not disclose sufficient information to enable or teach one skilled in the field of the invention to make and use the full scope of the claimed invention without undue experimentation for at least the following terms or phrases:

Claim	Term
All Asserted Claims	"a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate;"
All Asserted Claims	"a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region;"
All Asserted Claims	"the upper surface of Fin active region"
All Asserted Claims	"a contact region and a metal layer which are formed at said source/drain and gate contact region,"
Asserted Claims 1-6, 11, 12, 15–17	"the thickness of said gate oxide layer"
Asserted Claims 1-6, 11, 12, 15–17	"the thickness of said first oxidation layer"
Asserted Claims 2, 16, 17	"the width of said Fin active region"
Asserted Claims 3, 4	"the height of said Fin active region"
Asserted Claim 5	"the parasitic capacitance between said gate and bulk silicon substrate is reduced by selecting the thickness of said second oxidation layer to be between 20 nm and 800 nm."
Asserted Claim 6	"the contact resistance is reduced by selecting the size of a contact region which is in contact with said metal layer to be greater than the width of said Fin active region and/or the length of said gate."

Claim	Term
Asserted Claim 11	"said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to 50 nm above the reference level."
Asserted Claim 12	"said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to −50 nm below the reference level."
Asserted Claim 13	"the resistance of said Fin active region is reduced by enlarging the width of said Fin active region within the oxidation layer as it approaches the bulk silicon substrate."
Asserted Claim 15	"the two top corners of said Fin active region are chamfered through an oxidation and etching, or (and) annealing process in a hydrogen atmosphere."

To the extent other claims contain one or more of these terms or phrases, either directly or through being a dependent claim of a claim that does, those Asserted Claims of the Asserted Patent are invalid under 35 U.S.C. § 112, ¶ 1.

C. Lack of Written Description under 35 U.S.C. §112, ¶ 1

The Asserted Claims of the Asserted Patent are invalid because they fail to meet the "written description" requirement of 35 U.S.C. § 112, ¶ 1, because the Asserted Patent does not describe the limitations of the noted claims in sufficient detail that a person of ordinary skill in the art would recognize that the inventor possessed the full scope of the invention as later claimed at the time of filing for at least the following terms or phrases:

Claim	Term
All Asserted Claims	"a second oxide layer which is formed up to a certain height of the Fin active region from the surface of bulk silicon substrate;"

Claim	Term
All Asserted Claims	"a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region;"
All Asserted Claims	"the upper surface of Fin active region"
All Asserted Claims	"a contact region and a metal layer which are formed at said source/drain and gate contact region,"
Asserted Claims 1-6, 11, 12, 15–17	"the thickness of said gate oxide layer"
Asserted Claims 1-6, 11, 12, 15–17	"the thickness of said first oxidation layer"
Asserted Claims 2, 16, 17	"the width of said Fin active region"
Asserted Claims 3, 4	"the height of said Fin active region"
Asserted Claim 5	"the parasitic capacitance between said gate and bulk silicon substrate is reduced by selecting the thickness of said second oxidation layer to be between 20 nm and 800 nm."
Asserted Claim 6	"the contact resistance is reduced by selecting the size of a contact region which is in contact with said metal layer to be greater than the width of said Fin active region and/or the length of said gate."
Asserted Claim 11	"said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to 50 nm above the reference level."
Asserted Claim 12	"said doping junction depth for the source/drain formed in said Fin active region, when the upper surface of said second oxide layer is taken as a reference level (0 nm), is around 0 nm to −50 nm below the reference level."
Asserted Claim 13	"the resistance of said Fin active region is reduced by enlarging the width of said Fin active region within the oxidation layer as it approaches the bulk silicon substrate."

Claim	Term
Asserted Claim 15	"the two top corners of said Fin active region are chamfered through an oxidation and etching, or (and) annealing process in a hydrogen atmosphere."

To the extent other Asserted Claims contain one of these terms or phrases, either directly or through being a dependent claim of a claim that does, those Asserted Claims of the Asserted Patent are invalid under 35 U.S.C. § 112, ¶ 1.

Thus, the claims lack written description.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the foregoing document has been served on August 12, 2019, to all counsel of record via e-mail.

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